Amendments to the Specification

Please replace paragraph [0005] with the following amended paragraph:

[0005] Figure 2 illustrates the general architecture of a TDM switch. In general, the switch has a number of inputs and number of outputs. Data grains **102** received by ingress ports (not shown) are ordered as ingress grain ~~grains~~ groups **100**. The grains **102** are multiplexed by the switch **104** and transmitted by the egress ports (not shown) ordered as egress grain groups **106**. For illustrative purposes, the switching system illustrated in Figure 2 has N inputs and N outputs (NxN), but one skilled in the art will appreciate that a similar architecture can be implemented for asymmetrical switches. In Figure 2, grains **102** are labelled with a letter representing the input port and a number (ranging from 1 to G, the number of grains in the ingress grain group **100**) representing the byte position at the port. As can be seen in the output, bytes may be reordered to any position, may be multicast to several ports (or a single port), or may be dropped. Figure 2 shows switching of grains within one grain group. The same switching of grains is performed at all recurrences of the grain groups.